



# Intel® Programmable Services Engine (Intel® PSE) I/O Driver for Microsoft Windows\* 10 64-bit OS on Intel Atom® x6000E Series, Intel® Pentium® and Celeron® N and J Series Processors (Code Name: Elkhart Lake)

Release Notes

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## Revision History

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Date	Revision	Description
August 2021	1.2	MR1 Release
April 2021	1.1	Added support to Embedded SKU
March 2021	1.0	PV Release for PC Client and Industrial Non-FuSa SKU
January 2021	0.9	Pre-production QS Release
October 2020	0.8	Beta 3 Engineering Release
September 2020	0.7	Beta Release
July 2020	0.6	Alpha 2 Release
May 2020	0.5	Alpha Release
April 2020	0.3.1	Engineering Release #2
November 2019	0.3	Initial release

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## 1.0 Introduction

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This document provides release notes, driver interfaces, limitations, and known issues for the Intel® Programmable Services Engine (Intel® PSE) I/O driver binary packages for the Microsoft Windows\* 10 64-bit operating system.

### 1.1 Acronyms and Terminology

Table 1. Terminology

Term	Description
ACPI	Advanced Configuration and Power Interface
BKC	Best-Known Configuration
DMA	Direct Memory Access
GPIO	General-Purpose I/O
HECI	Host Embedded Controller Interface
IOCTL	I/O Control
IPC	Inter-process Communication
ODM	Original Design Manufacturing
OEM	Original Equipment Manufacturing
PIO	Programmed I/O
SoC	System on a Chip
SPB	Simple Peripheral Bus

### 1.2 Intended Audience

This document is intended for OEMs and ODMs that are enabling drivers with the Intel Atom® x6000E Series processors, Intel® Pentium® and Celeron® N and J Series processors.

### 1.3 Customer Support

Contact your Intel representative for support or submit an issue to Intel® Premier Support:

<http://premiersupport.intel.com>.

### 1.4 Reference Documents

Log in to the Resource and Design Center ([rdc.intel.com](http://rdc.intel.com)) to search for and download the document numbers listed in the following table. Contact your Intel field representative for an access.

**Note:** Third-party links are provided as a reference only. Intel does not control or audit third-party benchmark data or the web sites referenced in this document. You should visit the referenced web site and confirm whether the referenced data are accurate.

**Table 2. Reference Documents**

Document	Document No./Location
Best-Known Configuration (BKC) for Microsoft Windows* 10 RS5 (64-bit) OS on Intel Atom® x6000E Series Processors, Intel® Pentium® and Celeron® N and J Series Processors (Code name: Elkhart Lake)	<a href="#">616386</a>

## 2.0 Release Summary

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### 2.1 Hardware and Software Compatibility

This release is compatible with the following hardware:

- Intel Atom® x6000E Series, Intel® Pentium® and Celeron® N and J Series processors

This release supports the following operating system:

- Microsoft Windows\* 10 64-bit RS5 operating system

### 2.2 Release Contents

This release includes the following:

- Serial I/O drivers installer for Microsoft Windows\* 10 64-bit operating system:
  - I2C\* host controller driver (filename contains "iai2ce") version 40.100.2044.1
  - SPI host controller driver (filename contains "iaspie") version 40.100.2044.1
  - UART host controller driver (filename contains "iauarte") version 40.100.2044.1
  - HECI Controller driver (filename contains "ISH") version 5.4.1.4513
  - Intel® EC Lite Driver (filename contains "eclite") version 1.0.10099.248
- Intel® PSE I/O drivers for Microsoft Windows\* 10 release notes
- Intel Software License Agreement

## 3.0 Feature Highlights and Limitations

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### 3.1 I2C\* Host Controller Driver

Refer to the following link for details on the I2C\* SPB controller driver:

<https://docs.microsoft.com/en-us/windows-hardware/drivers/spb/spb-controller-drivers>

The driver binary package consists of the following files:

- iai2ce.inf
- iai2ce.cat
- iai2ce.sys

Enabled features are as follows:

- Supports 7-bit address modes
- Supports standard mode (100 Kbps), fast mode (400 Kbps), fast mode plus (1 Mbps), and high-speed mode (Max around 1.7 Mbps in PIO mode)
- Operates only on the primary mode
- Supports PIO and DMA transfer modes

**Limitation(s) are as follows:**

- PIO transfers at 1.4MHz and above may fail. Intel recommends enabling the DMA controller and using the default DMA mode for I2C high speed

### 3.2 SPI Host Controller Driver

Refer to the following link for details on the SPI SPB controller driver:

<https://docs.microsoft.com/en-us/windows-hardware/drivers/spb/spb-controller-drivers>

The driver binary package consists of the following files:

- iaspie.inf
- iaspie.cat
- iaspie.sys

Enabled features are as follows:

- Supports SPI modes 0, 1, 2, and 3
- Supports data bit length of 4 to 32
- Supports transfer rate of up to 5 Mbps in PIO mode
- Supports PIO and DMA transfer modes
- Operates only on the primary mode

**Limitation(s) are as follows:**

- Shared DMA for source and destination
- PIO transfers at 5MHz and above may fail. Intel recommends enabling the DMA controller and using the default DMA mode for SPI over 5MHz
- Transmit or receive only mode max speed 16.67MHz is verified. Full duplex mode max speed is limited under 8MHz in SPI driver because of DMA controller limitation. It needs the BIOS to allocate two channels from different DMA controllers to enable 16.67MHz full duplex transfer

### 3.3 UART Host Controller Driver

Refer to the following for details on the SerCx2 framework:

[https://msdn.microsoft.com/en-us/library/windows/hardware/hh439599\(v=vs.85\).aspx](https://msdn.microsoft.com/en-us/library/windows/hardware/hh439599(v=vs.85).aspx)

The driver binary package consists of the following files:

- iauarte.inf
- iauarte.cat
- iauarte.sys

Enabled features are as follows:

- Supports baud rates up to 6.25M
- Supports data sizes of 5, 6, 7, and 8 bits
- Supports none, odd, and even parities
- Supports 1, 1.5, and 2 stop bits
- Supports "Hardware" and "None" flow controls
- Supports full-duplex transmission and reception of data
- Supports PIO and DMA transfer modes
- Support wait events
- Support data transfer via serial terminal (The serial terminal/console application needs to support SerCx2 framework, e.g. Tera Term)

**Limitation(s) are as follows:**

- Shared DMA for source and destination
- If the DMA mode is turned on explicitly through the registry when the request is cancelled, the complete status or byte count may be incorrect. Suggest to use the default PIO mode

### 3.4 HECI Controller Driver

The Driver Binary Package consists of these files:

- ISH.inf
- ISH.cat
- ISH.sys

The following are the enabled features:

- Supports the HECI message over IPC for embedded controller communication.

**Limitation(s) are as follows:**

- No known limitation

### 3.5 Intel® EC Lite Driver

The Intel® EC Lite Driver conforms to the ACPI operation region and ACPI methods to pass the Intel® EC Lite Driver information to the ACPI methods related to the Windows\* energy management stack.

The Driver Binary Package consists of these files:

- eclite.inf
- eclite.cat
- eclite.sys

Enabled features are as follows:

- Supports pass information from the ACPI operation region to the Intel® PSE firmware
- Supports pass information from the Intel® PSE firmware to the ACPI operation region
- Supports asynchronous events from the Intel® PSE firmware
- Timeout for read request completion

**Limitation(s) are as follows:**

- No known limitation

### **3.6 Known Issues – Open**

Refer to the “Windows\* 10 Best Known Configuration on the Intel Atom® x6000E Series Processors, Intel® Pentium® and Celeron® N and J Series Processors (Document Number: [616386](#))” for the list of known issues.

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